ABSTRACT OF THE DISCLOSURE

A system for clock and data recovery ("CDR") includes a clock generator, a half-rate phase detector for receiving the input data, an encoder, a phase selector outputting recovered clock, a confidence counter, and a multiplexer outputting recovered data. The clock generator generates an 8-phase clock signal at half a rate of the transmitted serial data. The phase detector samples input data at four times the standard sampling rate, takes the oversampled data and detects phase transitions therein, i.e., phase lead and lag. The encoder encodes the phase transition data. The confidence counter receives the phase transition data and generates a signal representing the accumulated net effect of the phase transitions. The phase selector receives the confidence counter signal and the 8-phase clock from the clock generator, and determines the optimum phase for data sampling.